Amendments to the Specification

Please amend the Title as follows:

~~CIRCUIT ARRANGEMENT~~ TEST STRUCTURE FOR TESTING AN INTEGRATED CIRCUIT

On page 1, above line 1, insert the heading:

FIELD OF THE INVENTION

On page 1, between lines 3 and 4, insert the heading:

BACKGROUND OF THE INVENTION

On page 2, between lines 17 and 18, insert the heading:

SUMMARY OF THE INVENTION

On page 3, line 30, insert the heading:

BRIEF DESCRIPTION OF THE DRAWINGS

On page 4, line 4, insert the heading:

DETAILED DESCRIPTION OF THE INVENTION

Please amend the paragraph starting on page 4, line 27, as follows:

Furthermore, the control stage 10 comprises a first delay unit 24 which is connected to the output 22o of the first logic gate circuit 22 and delays the first clock signal C_1 by a first time interval Δt_1 (~~cf.~~ Fig. 1). A first D(elay)-flipflop unit 26 is connected to this first delay unit 24 and its clock input 26c is connected to the output 24o of the first delay unit 24 and the D input 26m is connected to the modulation signal input 12. In this way, the Q output 26o of the first D(elay)-flipflop unit 26 supplies the first modulation signal M_1, while the Q output 26o follows the signal of the D input 26m.

Please amend the paragraph starting on page 5, line 1, as follows:

Parallel thereto, the control stage 10 comprises a second delay unit 34 which is connected to the output 32o of the second logic gate circuit 32 and delays the second clock signal C_2 by a second time interval Δt_2 (~~cf.~~ Fig. 1). The first time interval Δt_1 and the second time interval Δt_2 have approximately equal temporal lengths (~~cf.~~ Fig. 2), while the first temporal delays Δt_1 generated in the first delay unit 24 and the second temporal delays Δt_2 generated in the second delay unit 34 can be built up, inter alia, with gate delay times.

Please amend the paragraph starting on page 5, line 15, as follows:

As is further evident from Fig. 1, the circuit arrangement 100 comprises a first driver stage 40 which is connected to a first power supply voltage $U_{dd,1}$ (~~cf.~~ Fig. 2)

amplitude-modulated by the first modulation signal M_1, and to a first reference potential $U_{ss,1}$ (= earth potential) and which can be impressed with the first clock signal C_1 in such a way that the output voltage $U_{o,1}$ of the first driver stage 40, which can be applied to the first terminal of the integrated circuit, temporally assumes the value of the amplitude-modulated first power supply voltage $U_{dd,1}$ and temporally the value of the first reference potential $U_{ss,1}$ (~~cf.~~ Fig. 2) in accordance with the clock of the first clock signal C_1.

Please amend the paragraph starting on page 5, line 23, as follows:

To this end, the first driver stage 40 has a clock signal input 42c provided for the first clock signal C_1, a modulation signal input 42m, provided for the first modulation signal M_1, for controlling the switching of the modulation voltage U_unmod or U_mod to the amplitude-modulated first power supply voltage $U_{dd,1}$ (~~cf.~~ Figs. 1 and 2), a first electronic switch 44 formed, for example, as a transistor, a second electronic switch 46 also formed, for example, as a transistor and ~~arranged behind~~ coupled to the first switch 44, and an output 48 provided for the first output signal comprising the output voltage $U_{o,1}$ (~~cf.~~ Fig. 2).

Please amend the paragraph starting on page 5, line 30, as follows:

In general, the function of the first driver stage 40 is based in this respect on the fact that – controlled by the clock of the first clock signal C_1 – each time one of the switches 44 and 46 becomes conducting so that the output 48 of the first driver stage 40

is alternately connected to the amplitude-modulated first power supply voltage $U_{dd,1}$ (modulation voltages ~~U_unmod/U_mod~~ U_unmod or U_mod, ~~cf.~~ Figs. 1 and 2) and to the first reference potential $U_{ss,1}$ (~~cf.~~ Fig. 2). The first temporal delay Δt_1 generated in the first delay unit 24 of the control stage 10 should be adjusted in such a way that the switching of the first power supply voltage $U_{dd,1}$ from the modulation voltage U_unmod to the modulation voltage U_mod always takes place when the second switch 46 of the first driver stage 40 is conducting.

Please amend the paragraph starting on page 6, line 5, as follows:

In order that the output voltage $U_{o,1}$ of the first driver stage 40, which output voltage can be applied to the first terminal of the integrated circuit, temporally assumes the value of the amplitude-modulated first power supply voltage $U_{dd,1}$ and temporally the value of the first reference potential $U_{ss,1}$ (~~cf.~~ Fig. 2) in accordance with the clock of the first clock signal C_1, the control means 442 of the first switch 44 and the control means 462 of the second switch 46 are connected to the clock signal input 42c of the first driver stage 40. The power supply voltage-sided contact 444 of the first switch 44 is connected to the amplitude-modulated first power supply voltage $U_{dd,1}$, whereas the reference potential-sided contact 464 of the second switch 46 is connected to the first reference potential $U_{ss,1}$. The output voltage-sided contact 446 of the first switch 44 and the output voltage-sided contact 466 of the second switch 46 are connected together and to the output 48 of the first driver stage 40.

Please amend the paragraph starting on page 6, line 16, as follows:

As is apparent from Fig. 1, the circuit arrangement 100 comprises a second driver stage 50 which is complementary to the first driver stage 40 and is connected to a second power supply voltage $U_{dd,2}$ (~~cf.~~ Fig. 2) amplitude-modulated by the second modulation signal M_2, and to a second reference potential $U_{ss,2}$ (= earth potential), and which can be impressed with the second clock signal C_2 in such a way that the output voltage $U_{o,2}$ of the second driver stage 50, which can be applied to the second terminal of the integrated circuit, temporally assumes the value of the amplitude-modulated second power supply voltage $U_{dd,2}$ and temporally the value of the second reference potential $U_{ss,2}$ (~~cf.~~ Fig. 2) in accordance with the clock of the second clock signal C_2.

Please amend the paragraph starting on page 6, line 25, as follows:

To this end, the second driver stage 50 has a clock signal input 52c provided for the second clock signal C_2, a modulation signal input 52m, provided for the second modulation signal M_2, for controlling the switching of the modulation voltage U_unmod or U_mod to the amplitude-modulated second power supply voltage $U_{dd,2}$ (~~cf.~~ Figs. 1 and 2), a first electronic switch 54 formed, for example, as a transistor, a second electronic switch 56 also formed, for example, as a transistor and ~~arranged behind~~ coupled to the first switch 54, and an output 58 provided for the second output signal comprising the output voltage $U_{o,2}$ (~~cf.~~ Fig. 2).

Please amend the paragraph starting on page 6, line 33, as follows:

In general, the function of the second driver stage 50 is based in this respect on the fact that – controlled by the clock of the second clock signal C_2 which is inverted with respect to the first clock signal C_1 – each time one of the switches 54 and 56 becomes conducting so that the output 58 of the second driver stage 50 is alternately connected to the amplitude-modulated second power supply voltage $U_{dd,2}$ (modulation voltages ~~U_unmod/U_mod~~ U_unmod or U_mod; ~~cf.~~ Figs. 1 and 2) and to the second reference potential $U_{ss,2}$ (~~cf.~~ Fig. 2). The second temporal delay Δt_2 generated in the second delay unit 34 of the control stage 10 should be adjusted in such a way that the switching of the second power supply voltage $U_{dd,2}$ from the modulation voltage U_unmod to the modulation voltage U_mod always takes place when the second switch 56 of the second driver stage 50 is conducting.

Please amend the paragraph starting on page 7, line 9, as follows:

In order that the output voltage $U_{o,2}$ of the second driver stage 50, which output voltage can be applied to the second terminal of the integrated circuit, temporally assumes the value of the amplitude modulated second power supply voltage $U_{dd,2}$ and temporally the value of the second reference potential $U_{ss,2}$ (~~cf.~~ Fig. 2) in accordance with the clock of the second clock signal C_2, the control means 542 of the first switch 54 and the control means 562 of the second switch 56 are connected to the clock signal input 52c of the second driver stage 50. The power supply voltage-sided contact 544 of the first

switch 54 is connected to the amplitude-modulated second power supply voltage $U_{dd,2}$, whereas the reference potential-sided contact 564 of the second switch 56 is connected to the second reference potential $U_{ss,2}$. The output voltage-sided contact 546 of the first switch 54 and the output voltage-sided contact 566 of the second switch 56 are connected together and to the output 58 of the second driver stage 50.

Please amend the paragraph starting on page 7, line 21, as follows:

As regards the embodiment of the circuit arrangement 100 shown in Figs. 1 and 2, the invention has the essential significance that the amplitude modulation is effected via the switching of the relevant power supply voltages $U_{dd,1}$ and $U_{dd,2}$ of the two driver stages 40 and 50, which power supply voltages $U_{dd,1}$ and $U_{dd,2}$ of the two driver stages 40 and 50 are switched at different instants because the first time interval Δt_1 and the second time interval Δt_2 have approximately equal temporal lengths. To this end, the two driver stages 40 and 50 are impressed with the mutually inverted, but symmetrical clock signals C_1 and C_2 so that two equally long clock phases [a] and [b] (~~cf.~~ Fig. 2) are produced at the outputs 48 and 58 of the driver stages 40 and 50, respectively.

Please amend the paragraph starting on page 7, line 30, as follows:

In clock phase [a] (~~cf.~~ Fig. 2) the relevant first switch 44, 54 is conducting and the relevant second switch 46, 56 is blocked so that the power supply voltages $U_{dd,1}$ and $U_{dd,2}$ are connected to the relevant outputs 48 and 58 of the driver stages 40 and 50,

respectively. In clock phase [b] (~~cf.~~ Fig. 2), the relevant first switch 44, 54 is blocked and the relevant second switch 46, 56 is conducting so that the reference potentials $U_{ss,1}$ and $U_{ss,2}$ are connected to the relevant outputs 48, 58 of the driver stages 40 and 50, respectively.

Please amend the paragraph starting on page 8, line 3, as follows:

As can be seen in Fig. 2, the first temporal delay Δt_1 generated in the first delay unit 24 and the second temporal delay Δt_2 generated in the second delay unit 34 are to be chosen in such a way that the first modulation signal M_1 and the second modulation signal M_2 switch the relevant power supply voltages $U_{dd,1}$ and $U_{dd,2}$ of the two driver stages 40 and 50 in the clock phase [b] in a secure manner (~~cf.~~ Fig. 2), in which clock phase the relevant power supply voltages $U_{dd,1}$ and $U_{dd,2}$ are not connected to the relevant outputs 48 and 58 of the driver stages 40 and 50, respectively. Since the two driver stages 40 and 50 operate with mutually inverted clock signals C_1 and C_2, the relevant instant of switching for the two driver stages 40 and 50 is different in this case (~~cf.~~ Fig. 2).